2016 International Conference
on Solid-State and Integrated Circuit Technology, Hangzhou, China
S59-3 Room 8
Oct. 28, 2016

Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator

Jun-ya Kojima Yukiko Arai Haruo Kobayashi

Gunma University, Japan

群馬大学
GUNMA UNIVERSITY

Research Objective

Objective

- **Development of high linear & high resolution ΔΣ DAC**

Our Approach

- **Limit cycle suppression using digital dither**

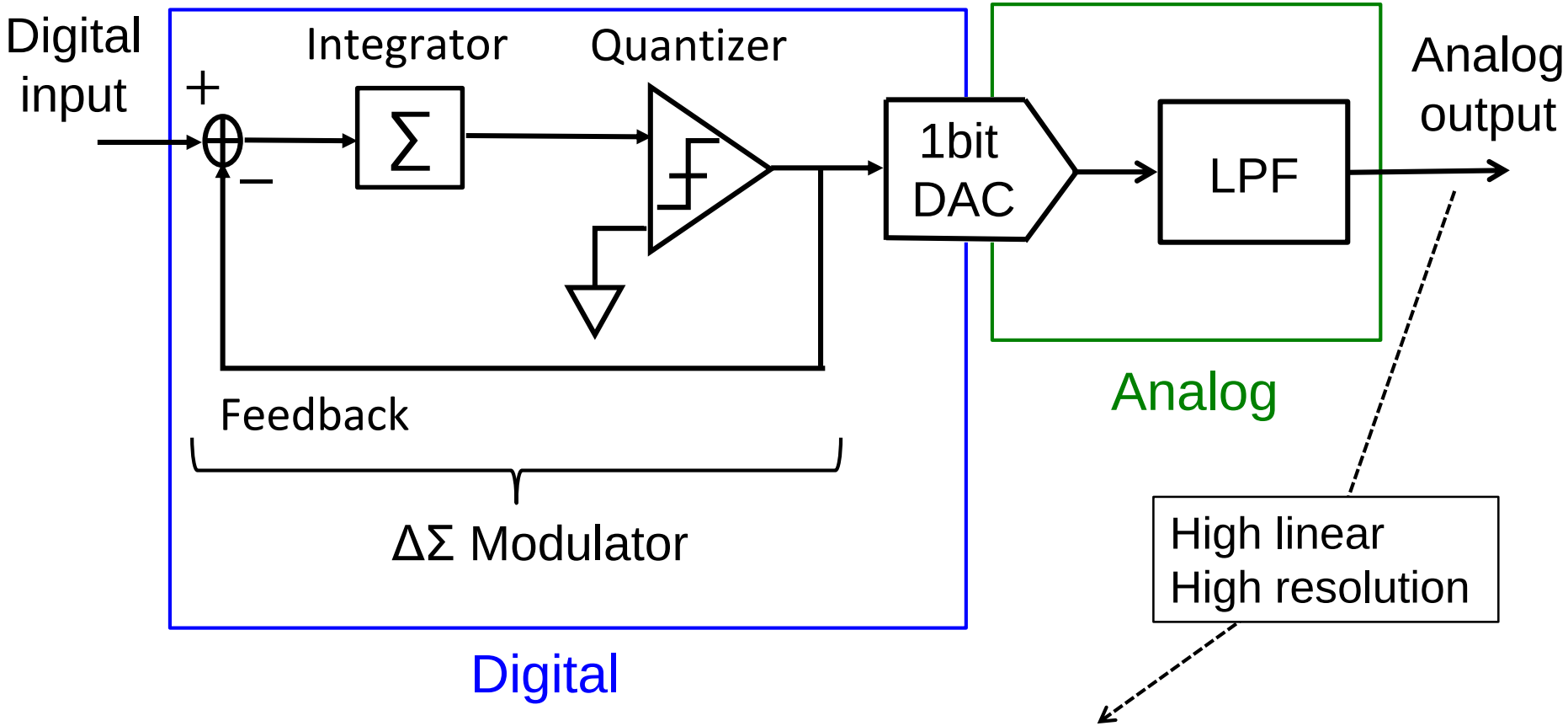
Outline

- Research Background
- Proposed Circuit
- Simulation Configuration & Results
- FPGA Implementation
- Conclusion

Outline

- **Research Background**
- Proposed Circuit
- Simulation Configuration & Results
- FPGA Implementation
- Conclusion

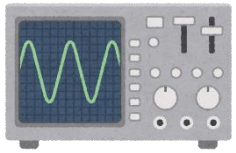
ΔΣ DA Converter



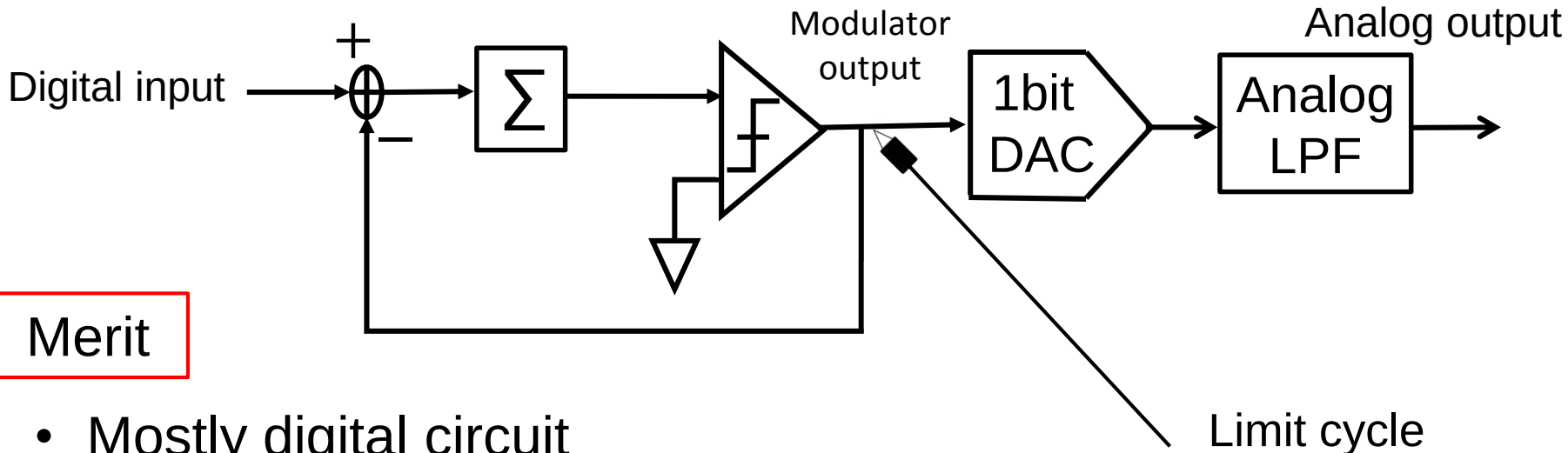
High linear
High resolution

＜Usage＞

- Measurement
- Audio



Merits & Demerits of ΔΣ DAC



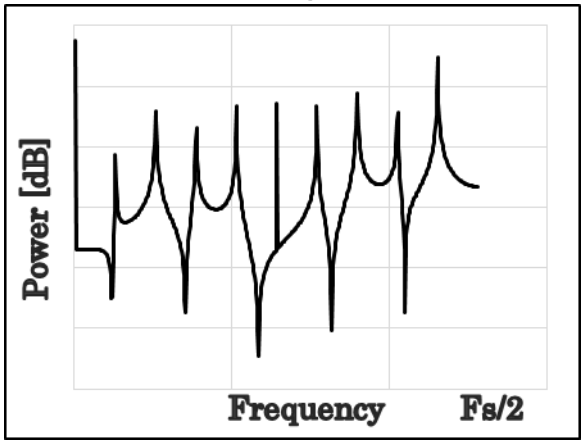
Merit

- Mostly digital circuit
- High linear & high resolution
  for low frequency signal generation

Demerit

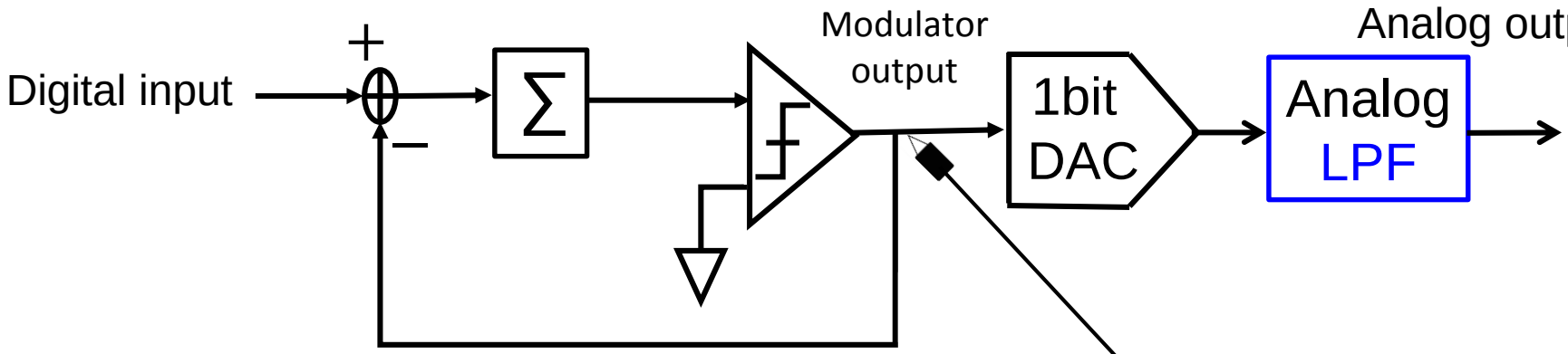
- Limit cycle problem for small input

Limit cycle



※ Due to modulator nonlinearity by quantizer

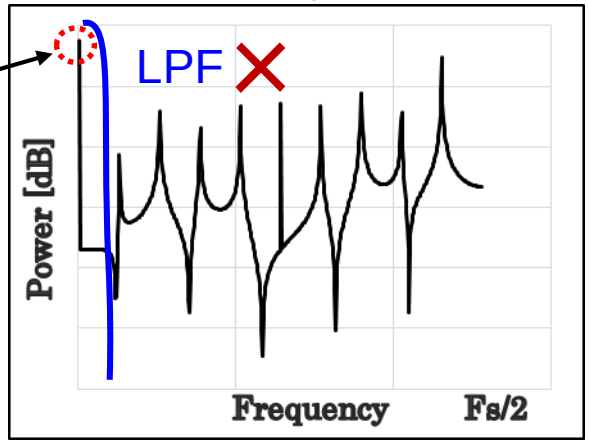
Limit Cycle Problem



Removal of analog signal by LPF sharply

⇒ difficult

Limit cycle

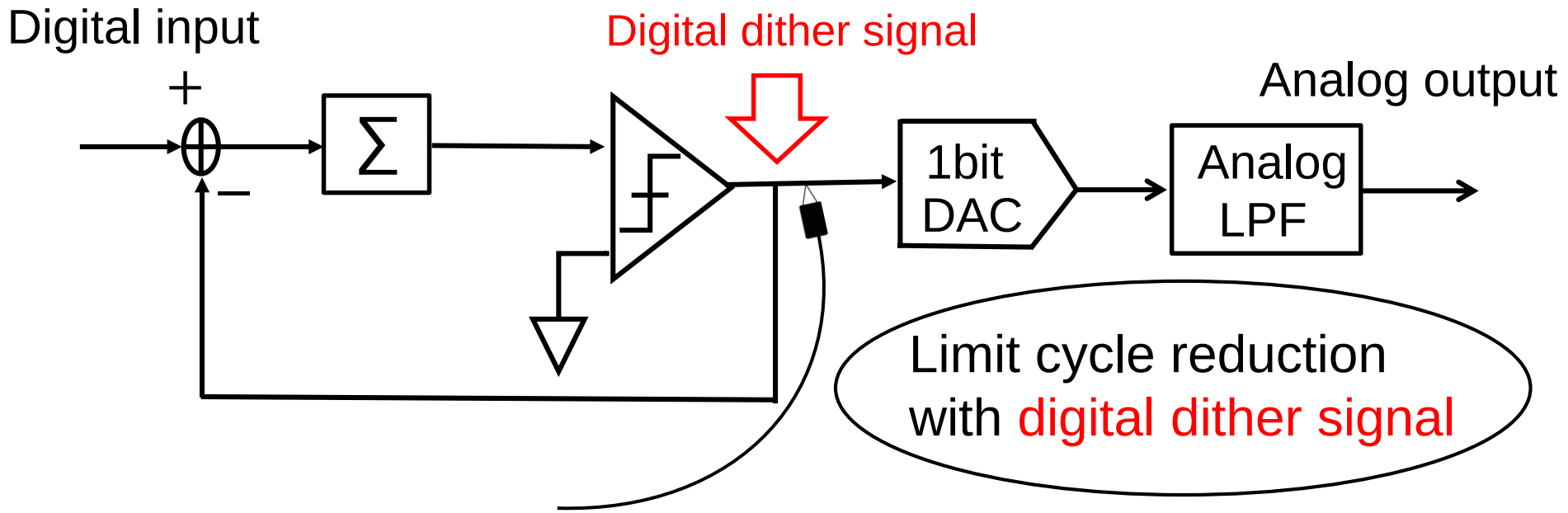


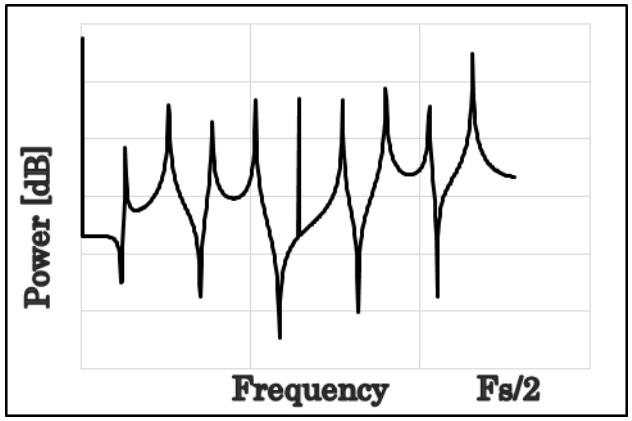
Analog output = Signal + Limit cycle

(Noise)

Objective
- Limit cycle suppression
- Relax LPF requirement

Our Approach





Limit cycle

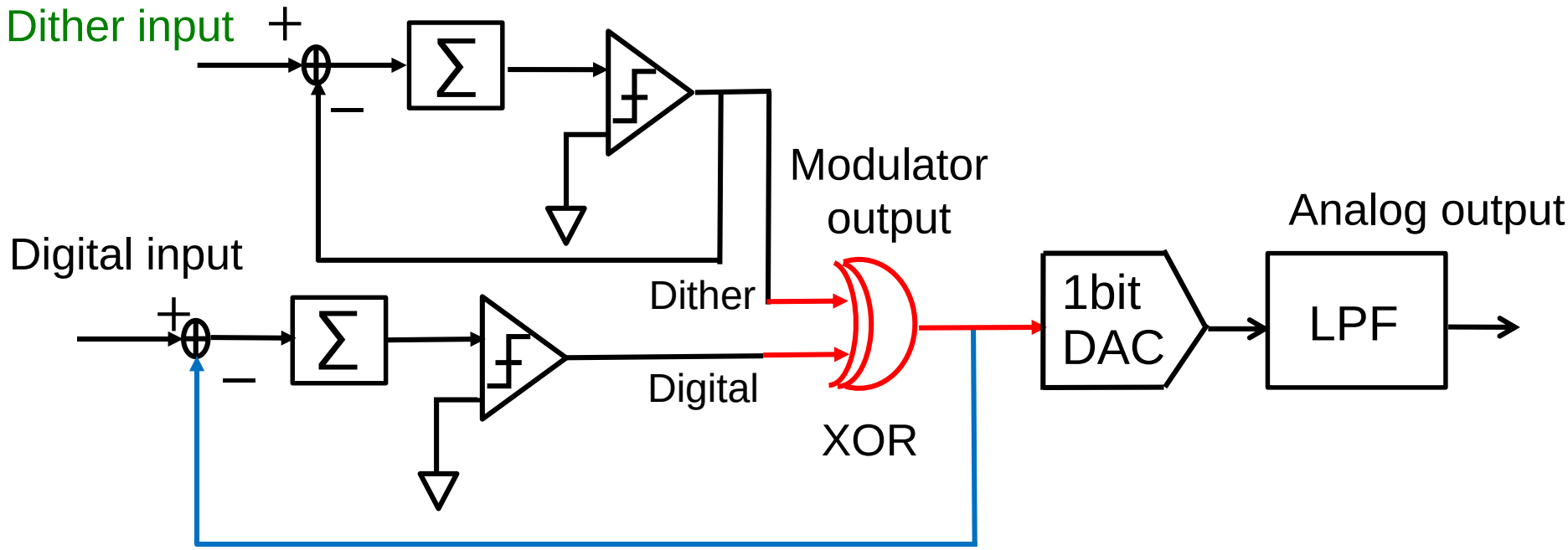
Stair

Smoothness !

Outline

- Research Background
- **Proposed Circuit**
- Simulation Configuration & Results
- FPGA Implementation
- Conclusion

Proposed Circuit



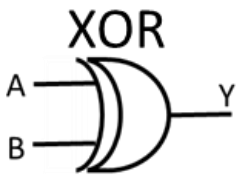
< Features >

① 1-bit output

② Digital dither

⇒ NOT affect output signal, thanks to feedback

③ Easily generated digital dither



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

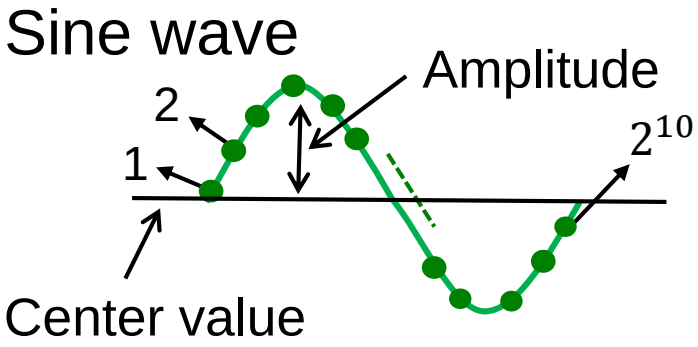
Digital signal “1” reverses comparator output with XOR

Outline

- Research Background
- Proposed Circuit
- **Simulation Configuration & Results**
- FPGA Implementation
- Conclusion

Simulation Configuration

◆ In 10-bit case



Amplitude and center value

➡ Controlled by number of 1's

Digital dither signal

Dither signal

Modulator output

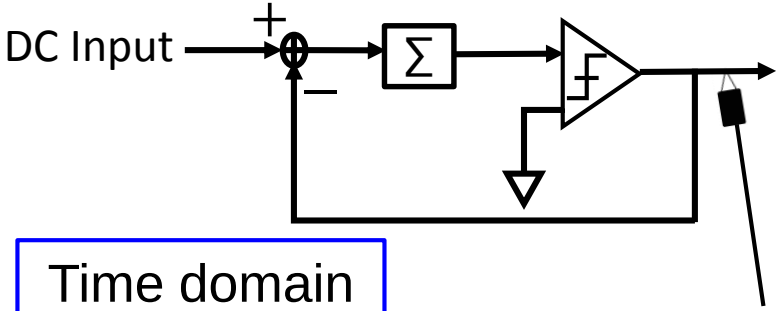
Digital signal

DC: -1～+1

「0」or「1」

Modulator Operation

- Without dither

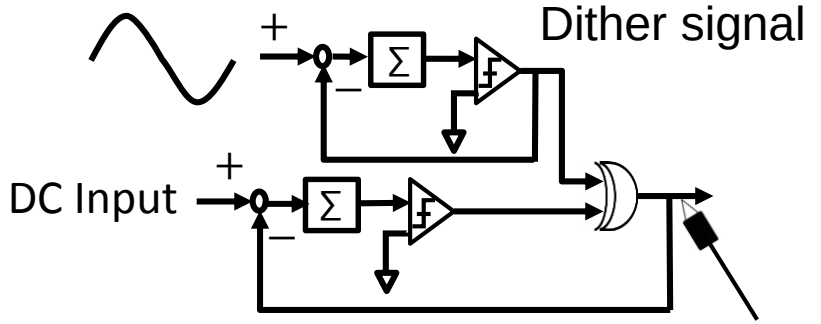


Time domain

1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0

Period

- With dither



1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

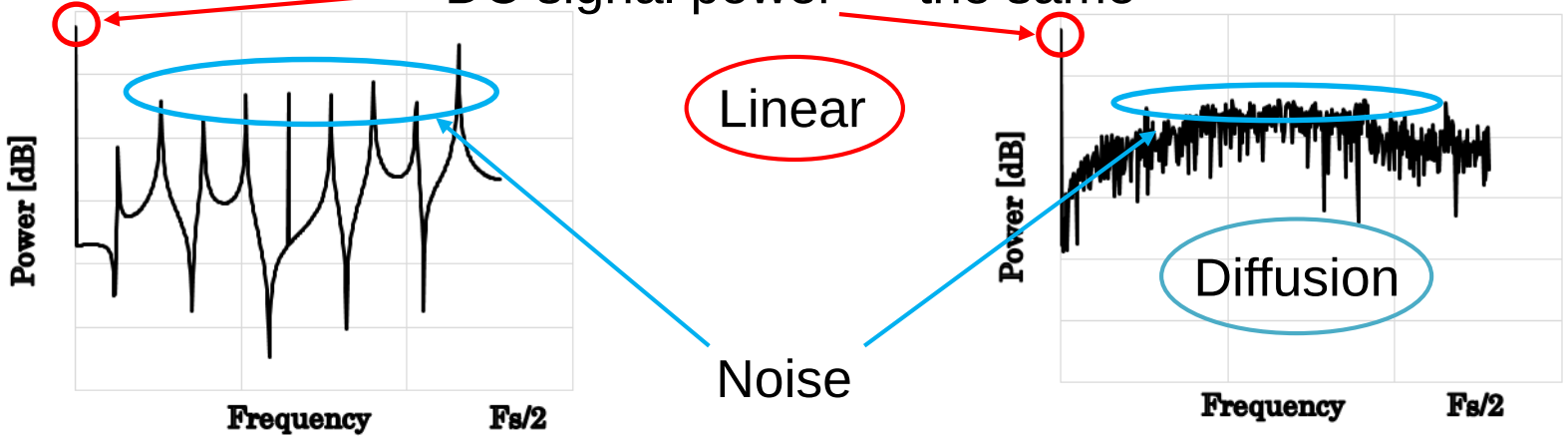
Not Periodic

✓ Orders of ‘0’ and ‘1’ ⇒ different

✓ Total numbers of 1’s ⇒ the same

Frequency domain

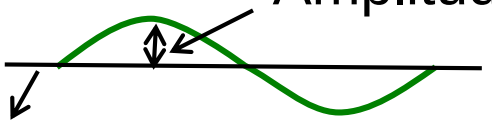
DC signal power ⇒ the same



10-bit case

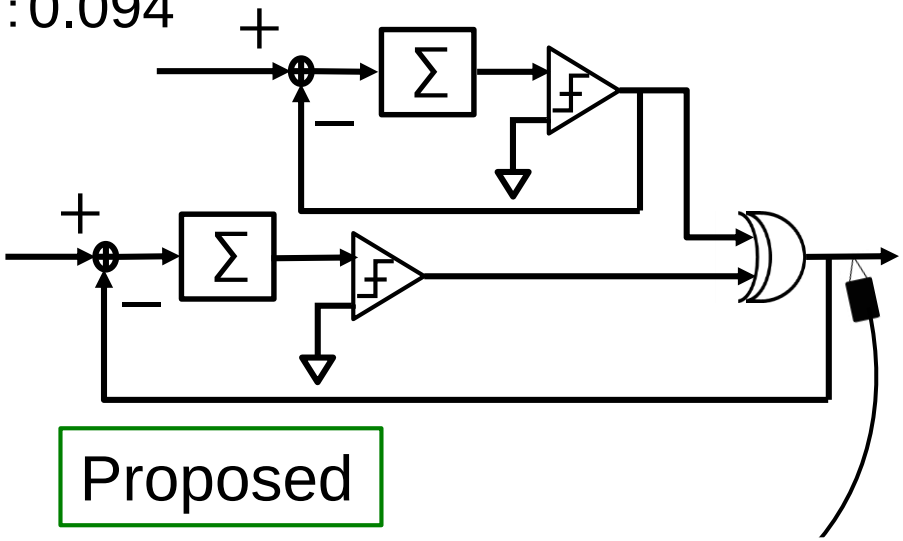
Simulation Results

Sine wave

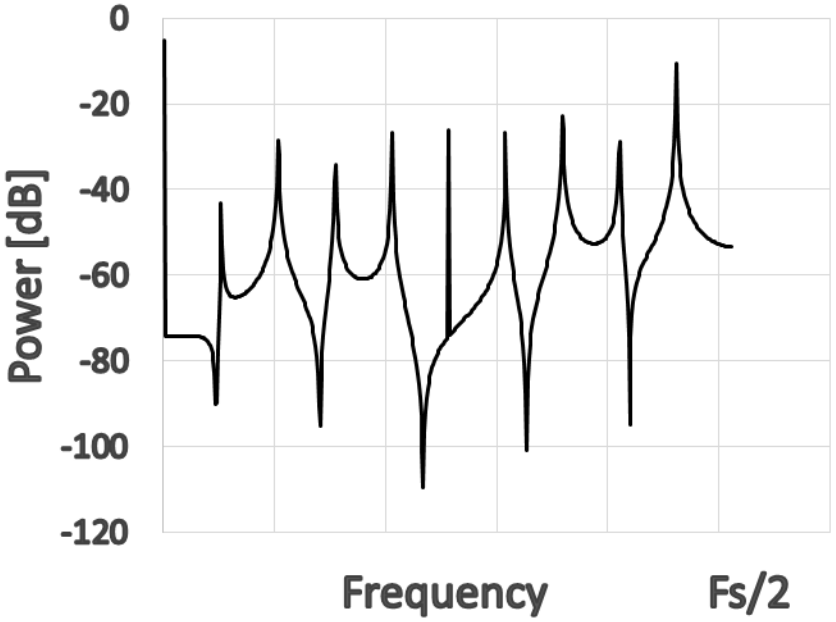


Center value : -0.520

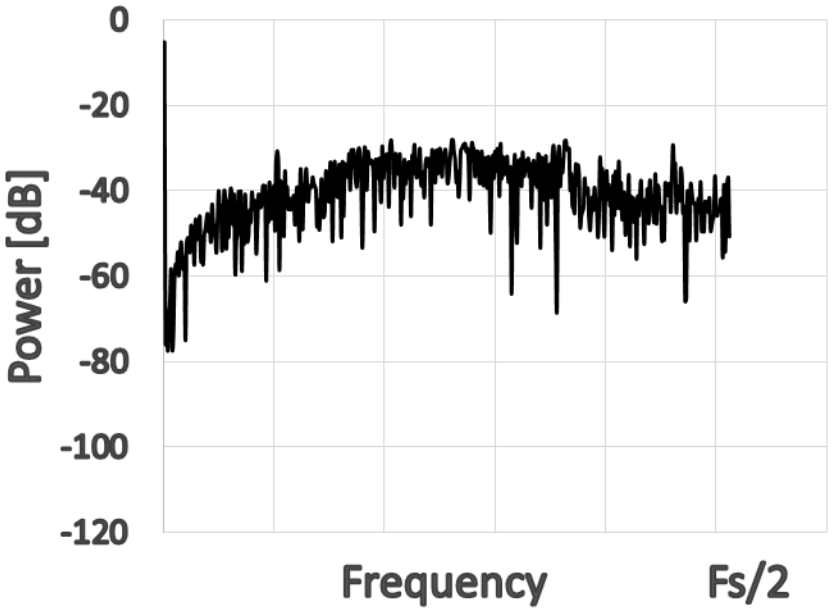
DC = 0.1



Conventional



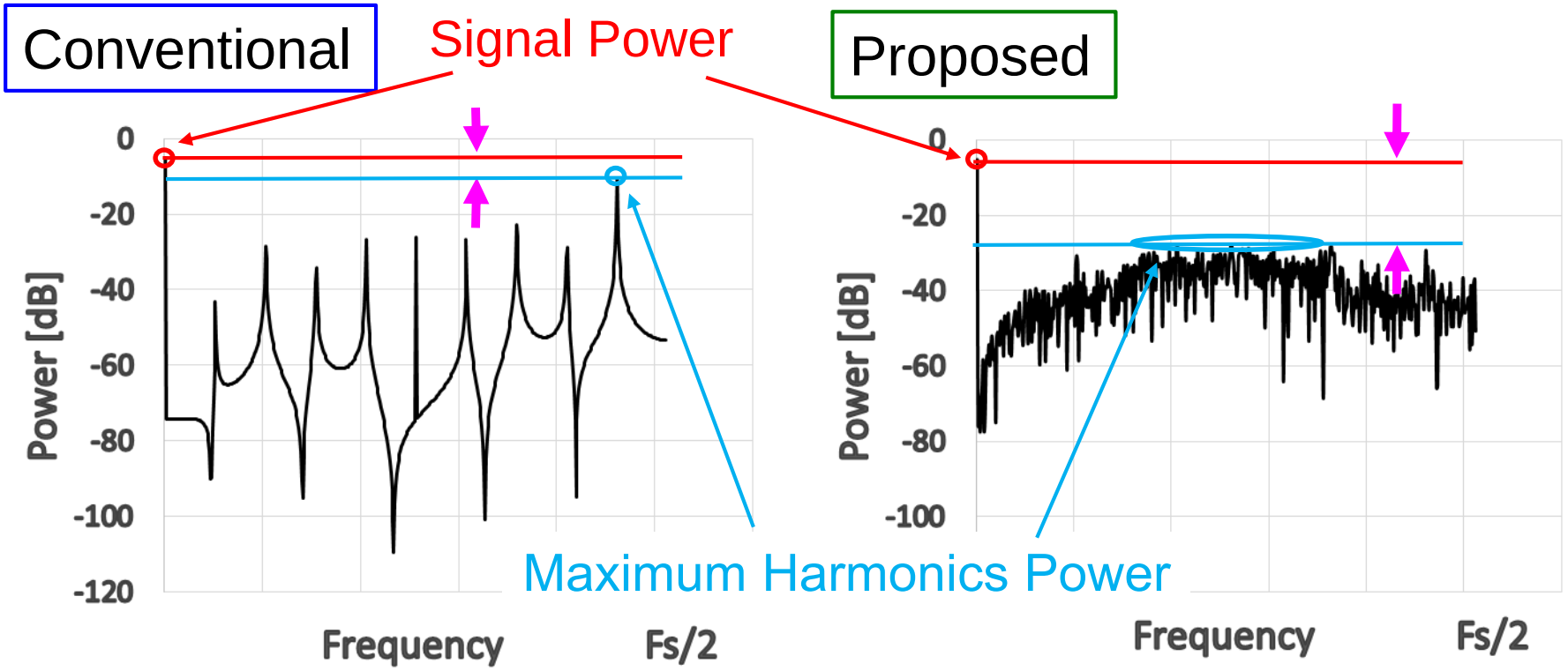
Proposed



SFDR (Spurious Free Dynamic Range)

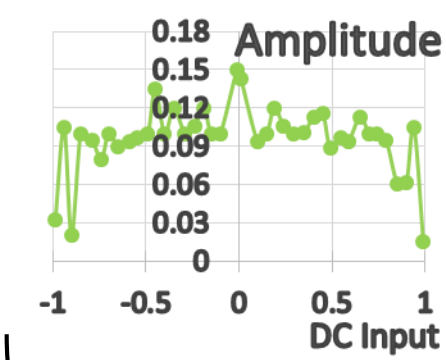
$$\mathrm{SFDR} = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

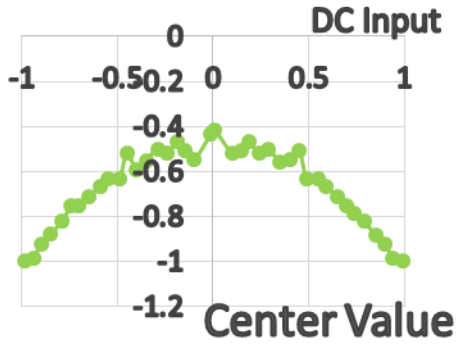
SFDR = 5.4 dB ＜ 22.9 dB

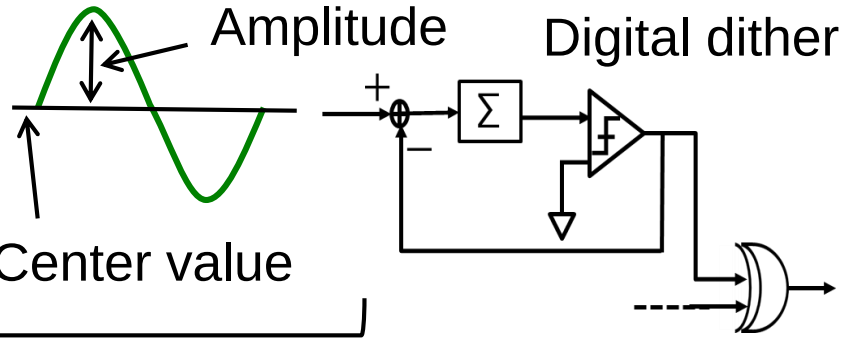


10-bit case

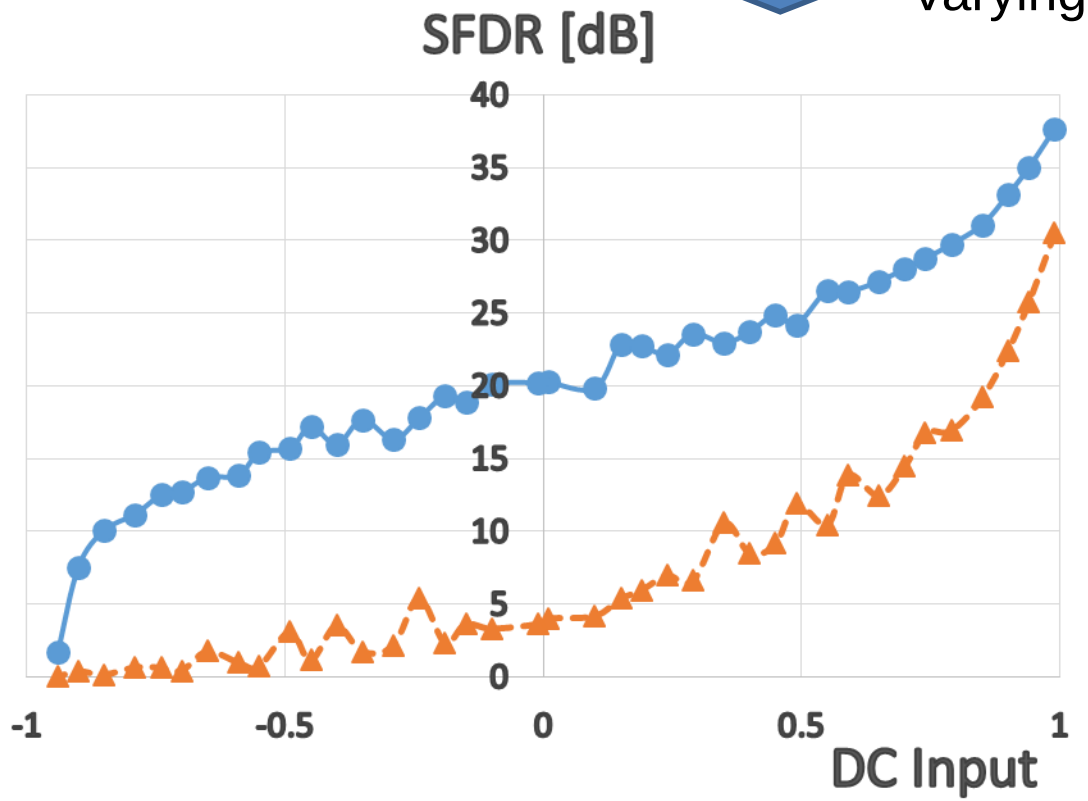
SFDR Comparison







Varying DC input



With dither
Without dither

SFDR improvement
by more than 10dB

Outline

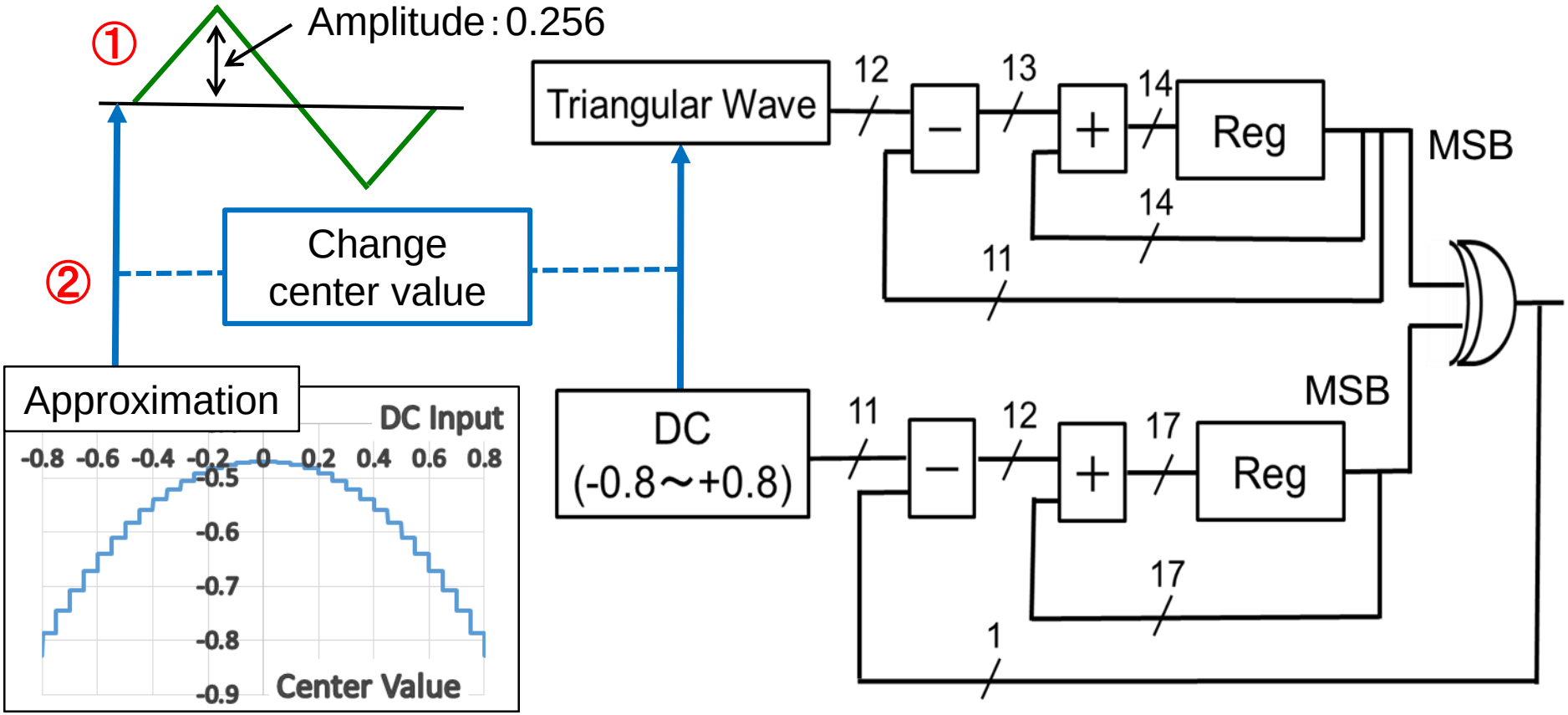
- Research Background
- Proposed Circuit
- Simulation Configuration & Results
- **FPGA Implementation**
- Conclusion

Design Modification for FPGA Implementation

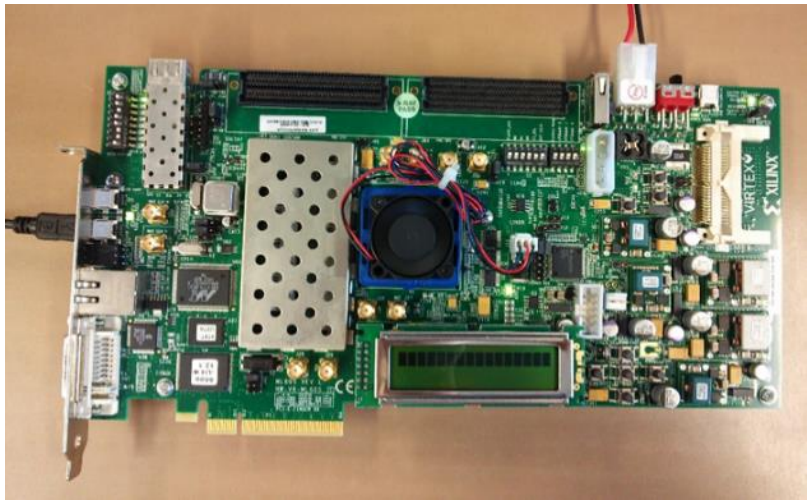
Complication

① Digital sine wave
⇒ Triangular wave

② Change amplitude and center value
⇒ Use approximation



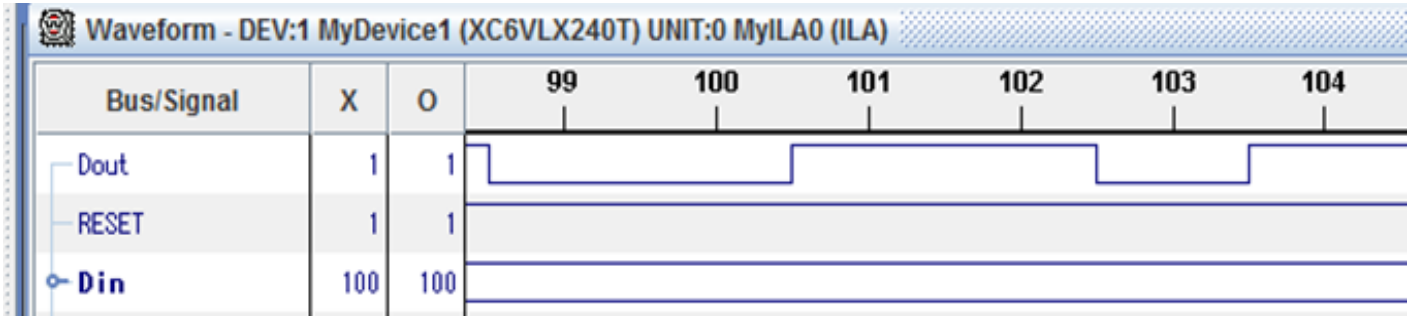
FPGA Board & Output Signal Waveforms



Xilinx
Virtex-6 ML605

FPGA Board

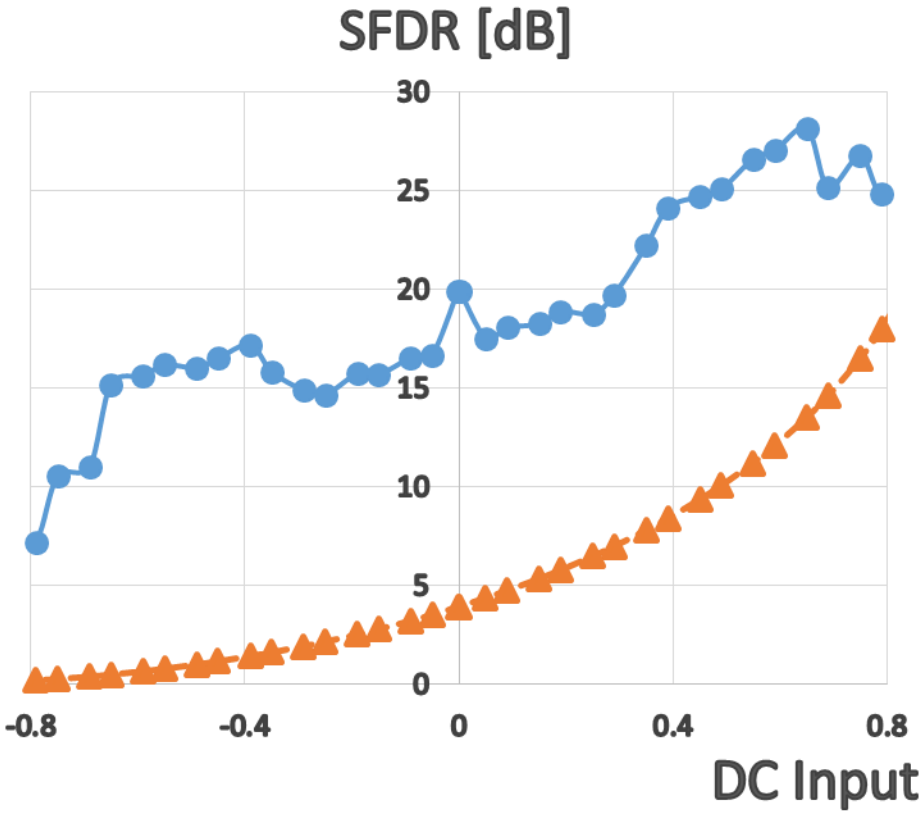
(Clock Freq. 50MHz)

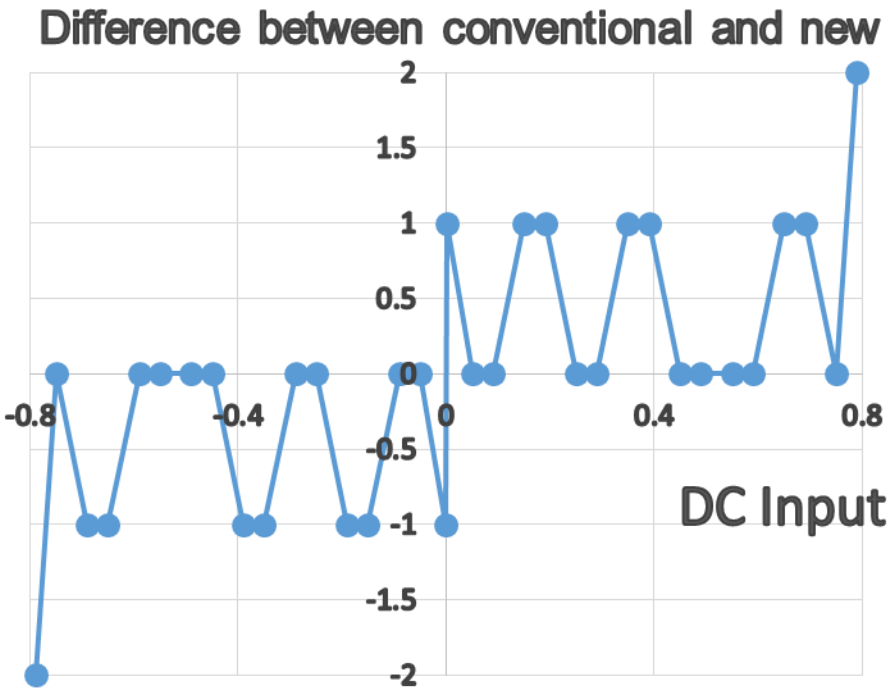


Part of output waveforms

FPGA Measurement Results

- 10-bit case





Difference between numbers of 1's
⇒ within ± 2
(※Total number is 1024)

SFDR improvement
⇒ more than 10dB

⇒ Linear DC

Outline

- Research Background
- Proposed Circuit
- Simulation Configuration & Results
- FPGA Implementation
- **Conclusion**

Conclusion

＜ ΔΣ DA modulator ＞

Conventional：Limit cycle problem for small input

Proposed：Using digital dither

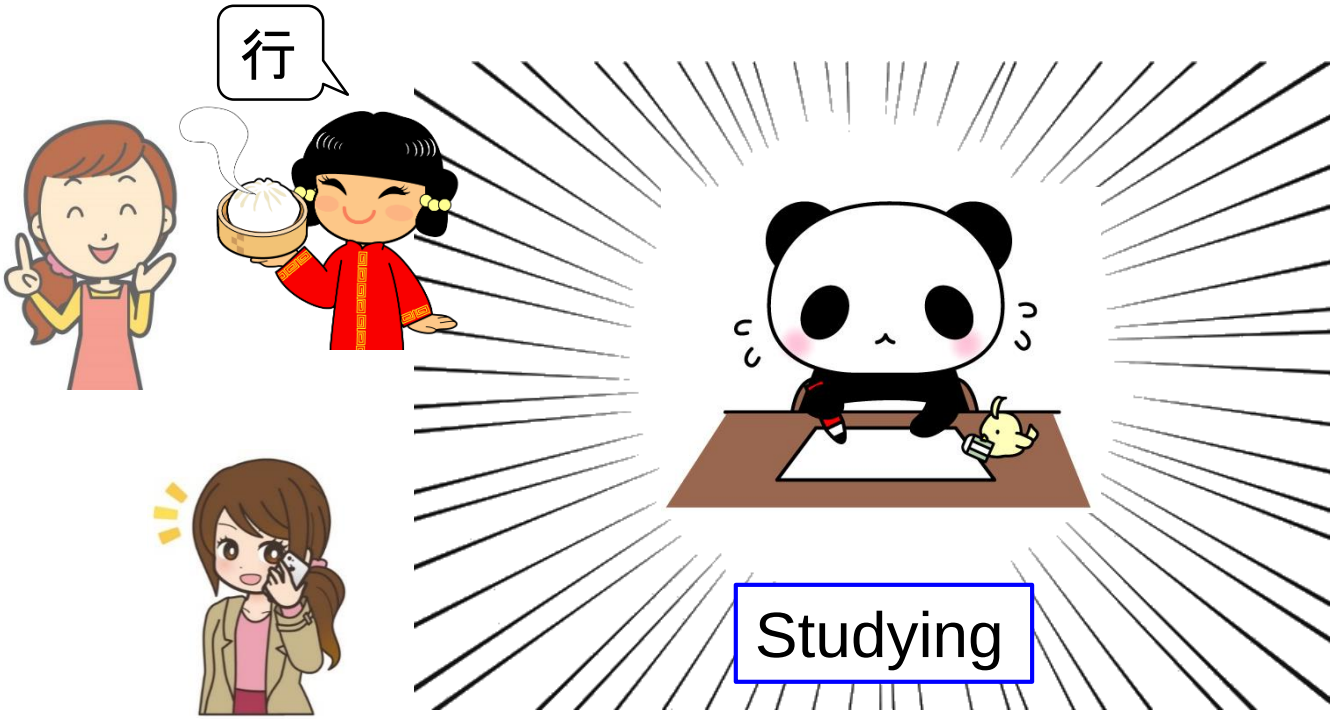
- Limit cycle reduction ⇒ Relax LPF requirement
- SFDR improvement by 10 dB
- Linear DC
- 1-bit DAC following a modulator thanks to XOR
- FPGA implementation

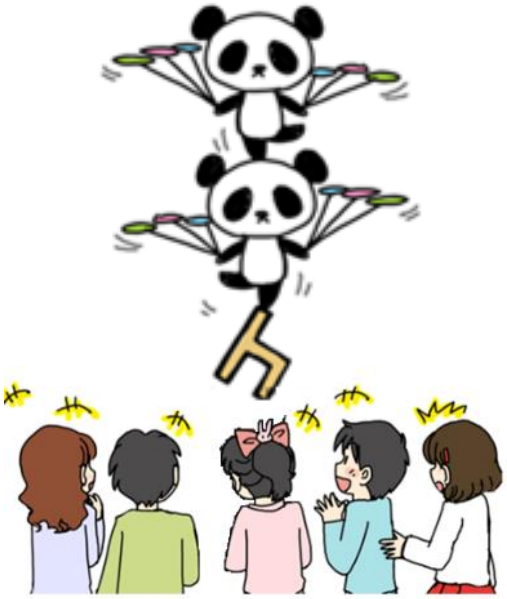
Human & Circuit are the Same

We can NOT concentrate
at completely quiet place

Philip E. Vernon
British Psychologist

Small ‘noise’ is good environment



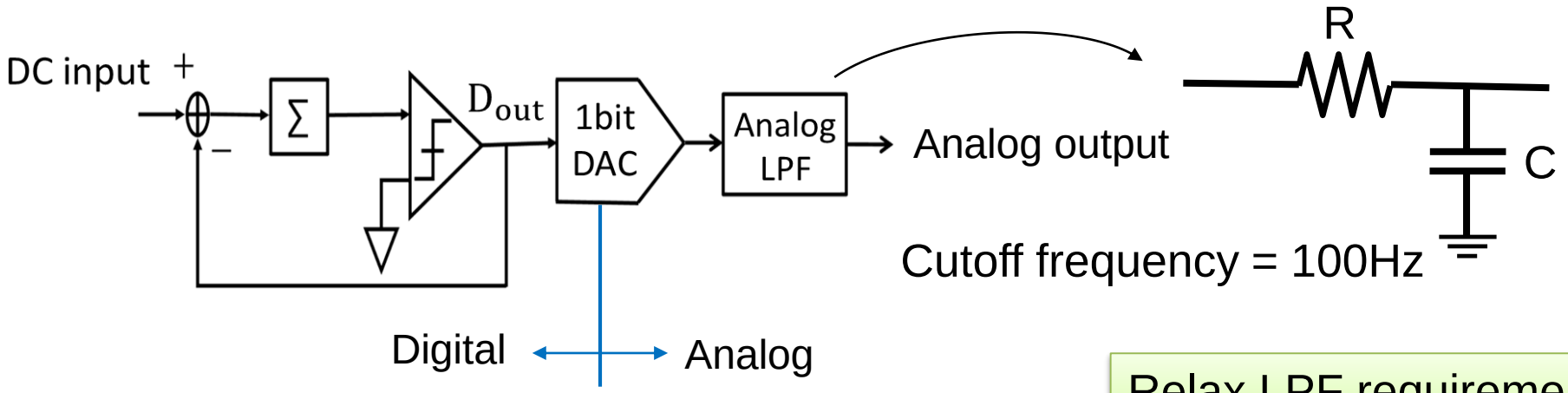


Appendix

App.

10-bit case
DC = 0.1

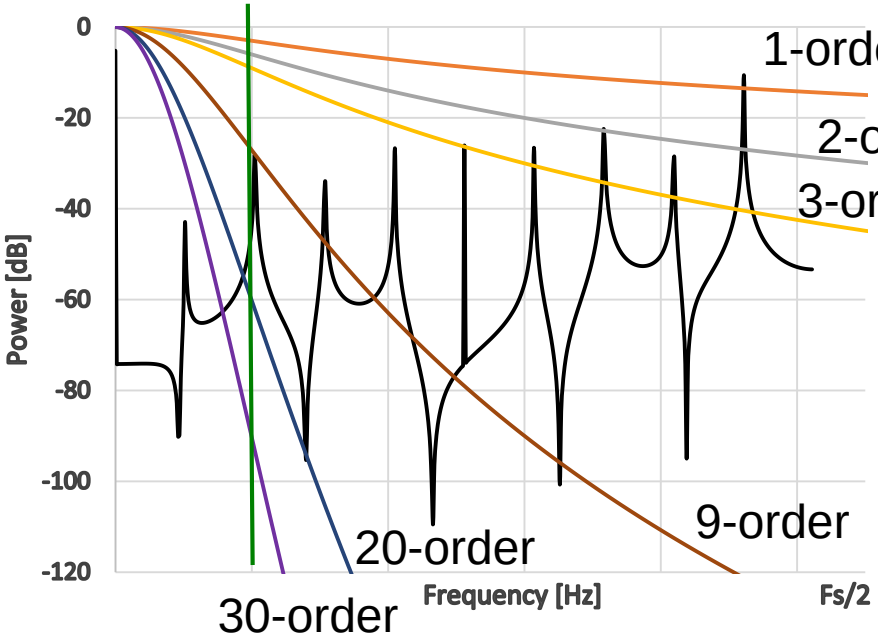
Latter LPF



Relax LPF requirement

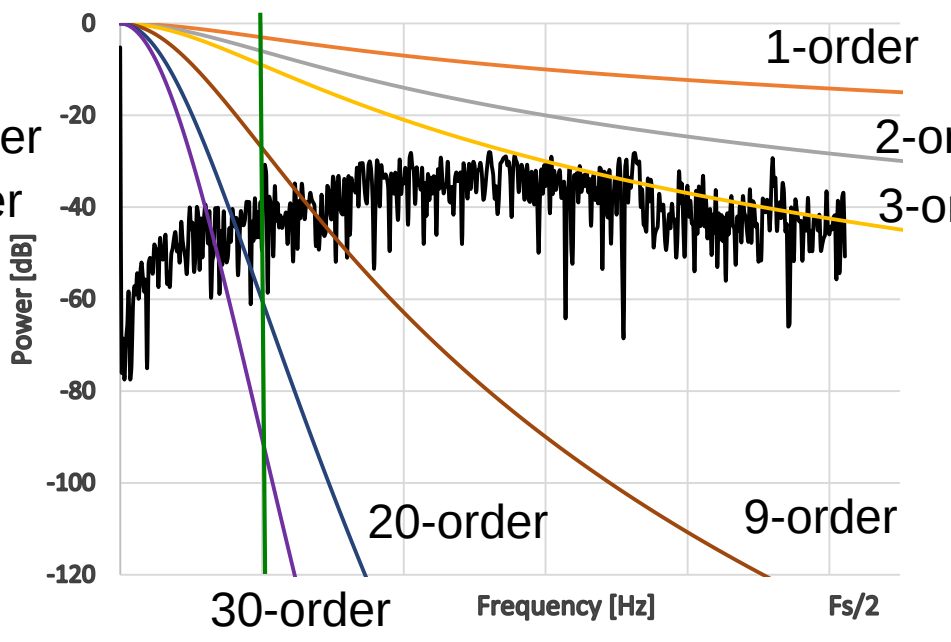
Conv.

f = 100Hz



Prop.

f = 100Hz

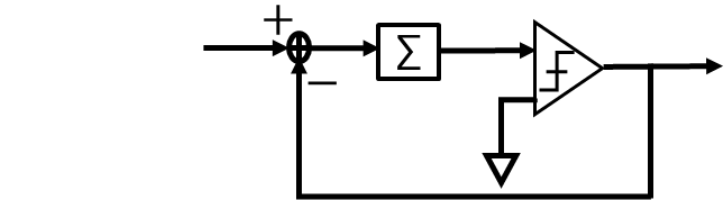


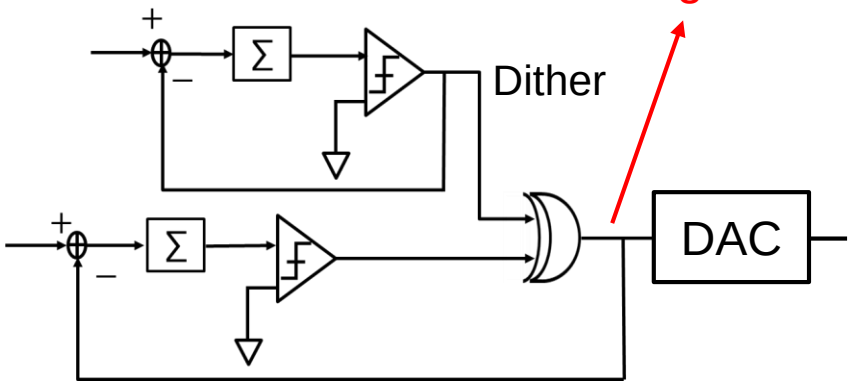
Using XOR gate

- Proposed circuit

Using XOR gate

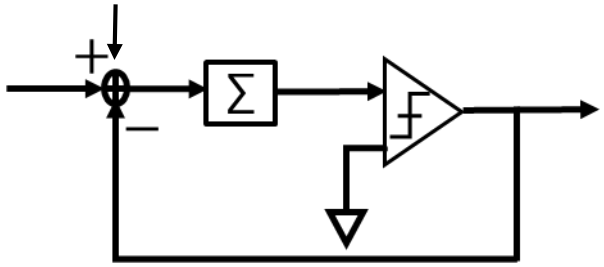
The conventional





- Input dither before ΔΣ modulator

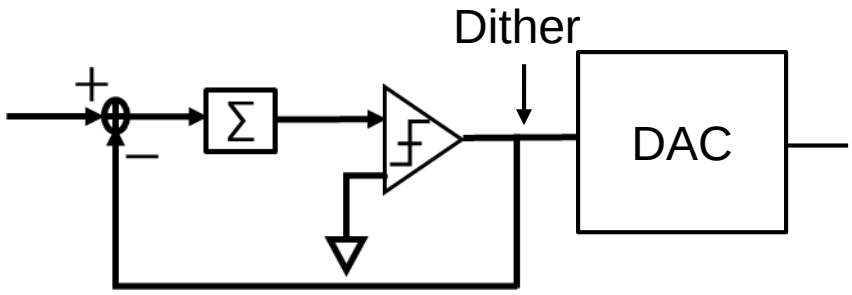
Dither



Increased noise

due to dither adds quantization error

- Input dither after ΔΣ modulator



Multi-bit DAC

Q1:なぜディザ入力信号に1Hzの正弦波を入力したが、
なぜ1Hzにしたのか？

A1: Because the sine wave of 1Hz is very simple. Also, I think I do not want to input the larger noise.

Q2:どのようにして最適な振幅、中心値を決めたのか？

A2:I determine the amplitude and the center value for maximum SFDR.

Q3:SFDRで評価しているが、後段にLPFがあるのでリミットサイクルは低周波側のみを評価するべきではないか。なぜ、高周波側で評価しているのか。

A3:Because relax the most of LPF requirement.
In addition, SFDR is simple indicator, and can apply the various signal bands, such as DC.

Q4:量子化器で出力された「0」または「1」をXORで反転させるのは、とても大きなディザ(ノイズ)を入れていると思うのだが大丈夫なのか。小さいディザの方が小さい誤差となるのではないのか。

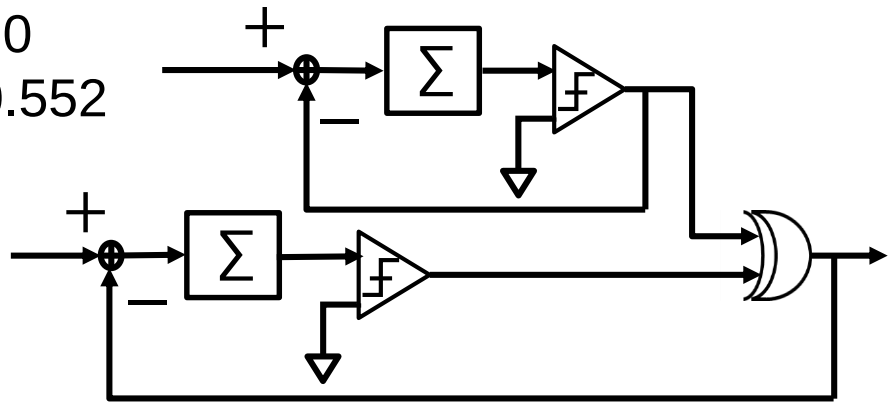
A4:The modulator output of the proposed is the same as that of the conventional.
So, the proposed circuit has no problem.

Some audio systems have the limit cycle in the signal band.
So, the limit cycle cannot be removed by LPF.
It is necessary to reduce the limit cycle in advance.

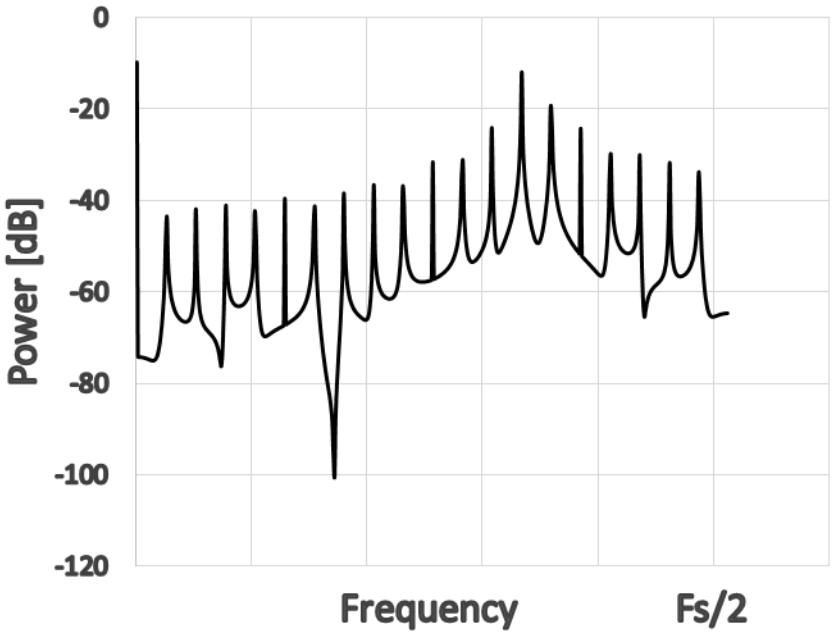
Simulation Results 10-bit case

Sine Wave Amplitude : 0.120
Center Value : -0.552

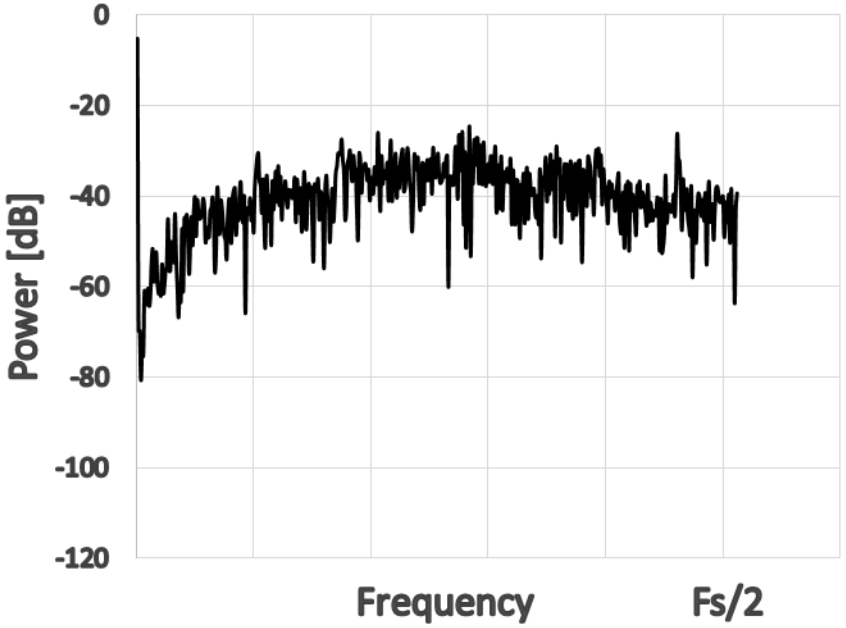
DC = -0.35 V



Conventional



Proposed



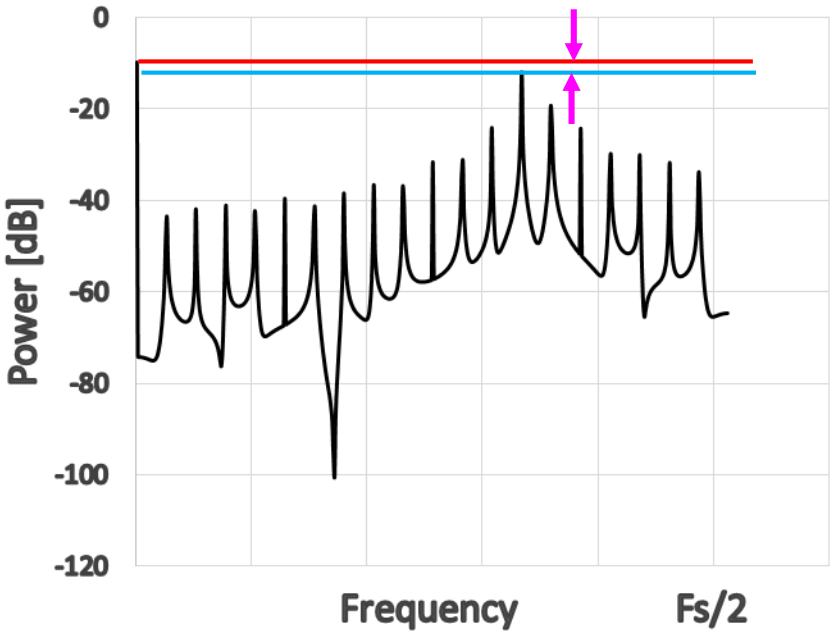
Simulation Results

10-bit case
DC = -0.35

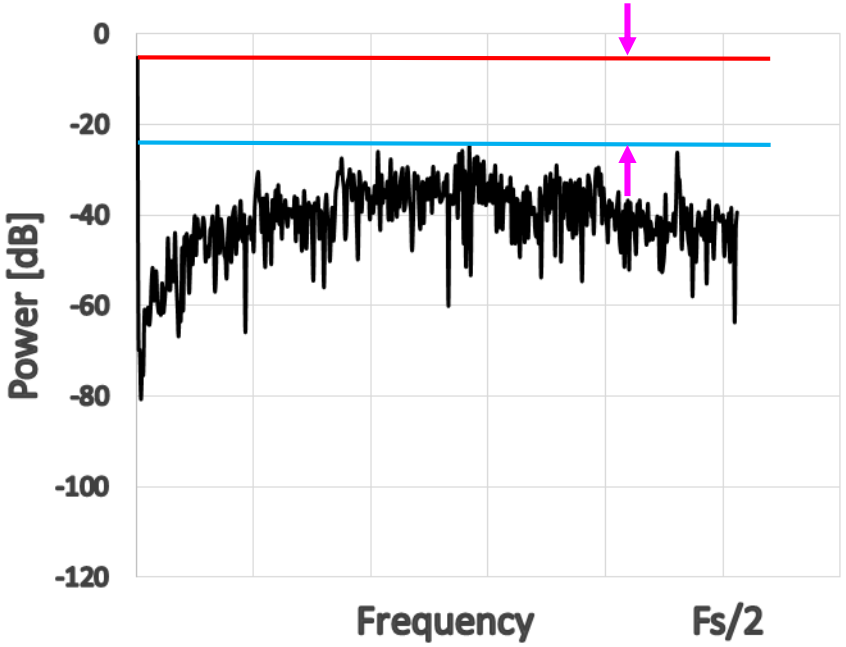
$$SFDR = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

SFDR = 2.16 dB < 16.33 dB

Conventional

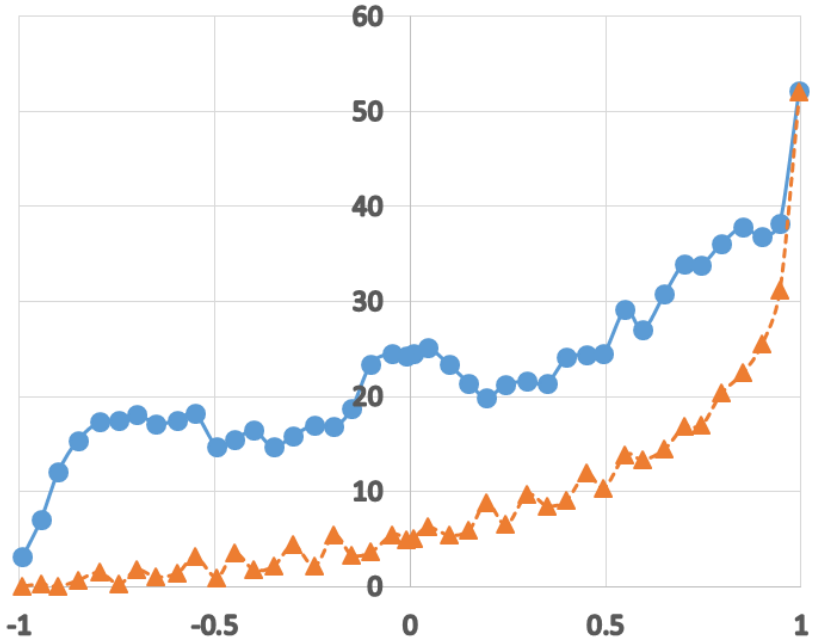


Proposed



Simulation Results 14-bit case

SFDR [dB]

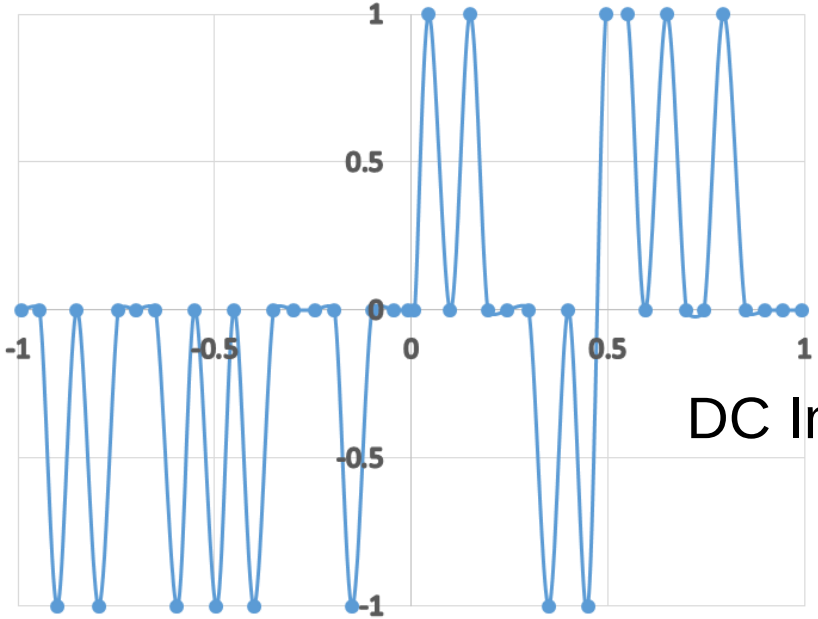


With dither
Without dither

DC Input

SFDR improvement
⇒ more than 10dB

Difference between conventional and new



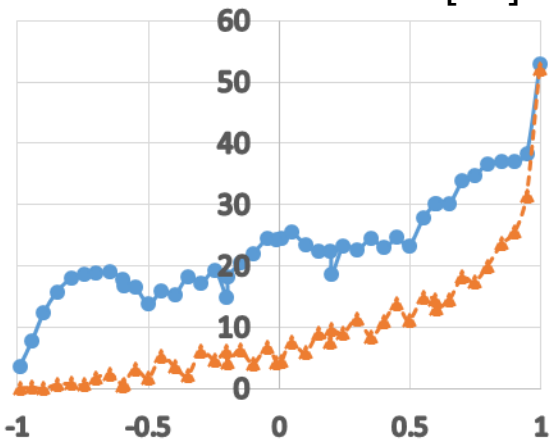
DC Input

Difference between numbers of 1's
⇒ within ± 1
(※Total number is 16384)

Linear DC

Simulation Results

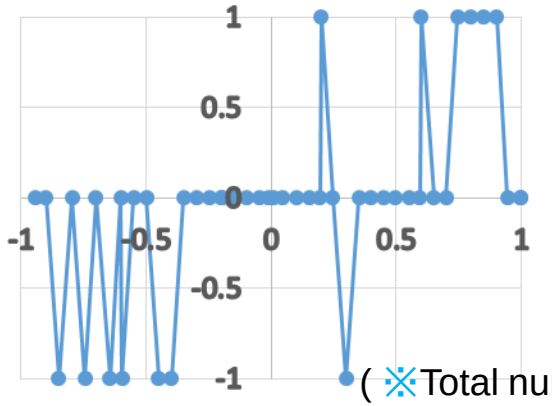
SFDR [dB]



DC Input

16-bit

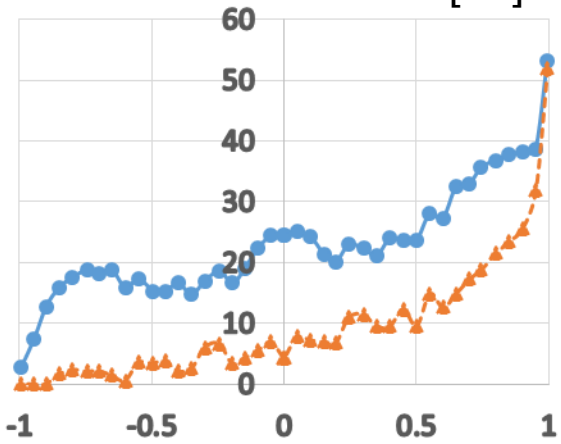
Difference between conventional and new



DC Input

(※Total number is 65536)

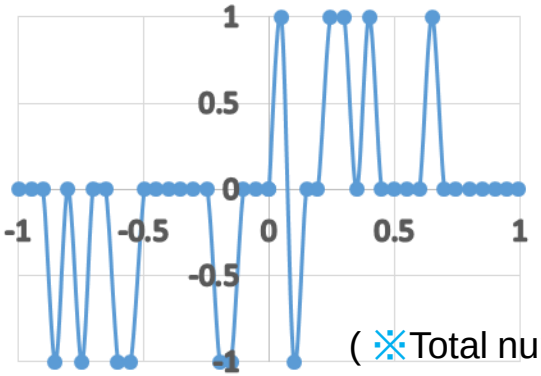
SFDR [dB]



DC Input

18-bit

Difference between conventional and new



DC Input

(※Total number is 262144)

With dither — Without dither - - -

Difference between numbers of 1's

⇒ within ± 2

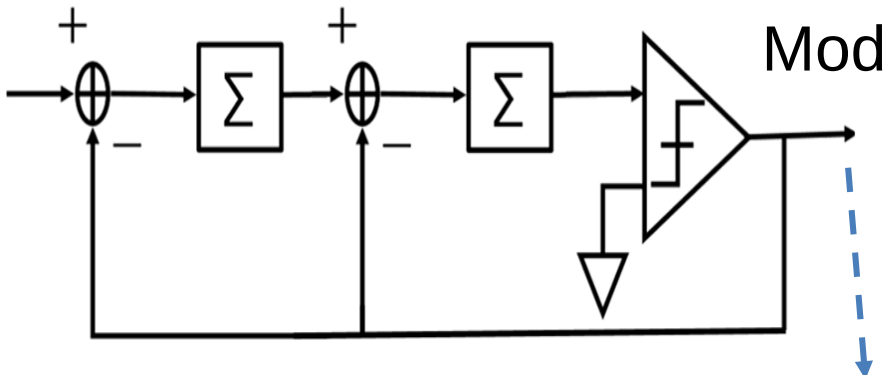
SFDR improvement ⇒ more than 10dB

⇒ Linear DC

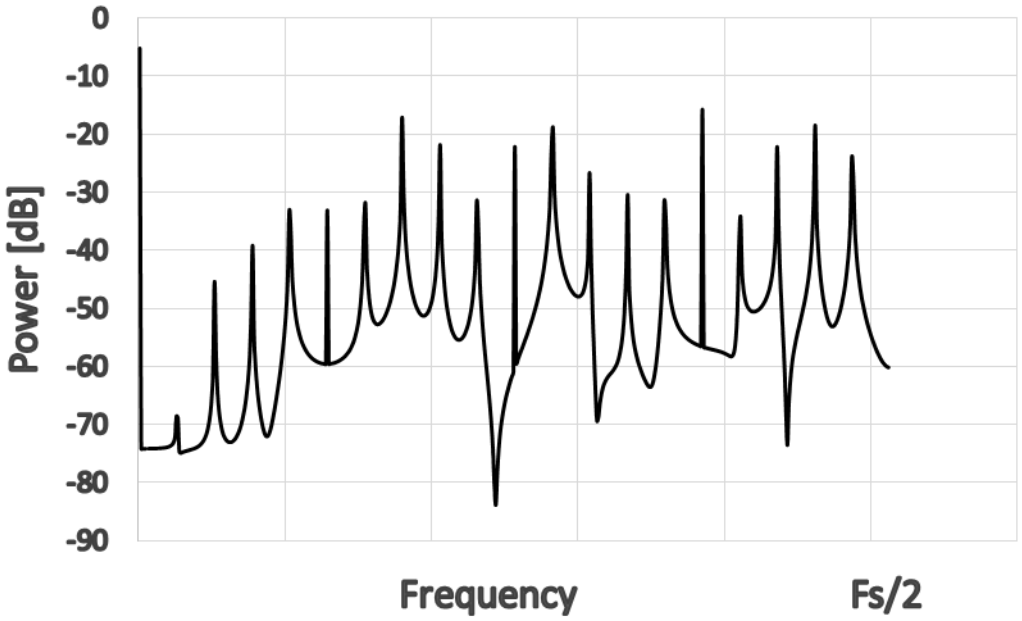
Second-Order ΔΣ modulator

10-bit case

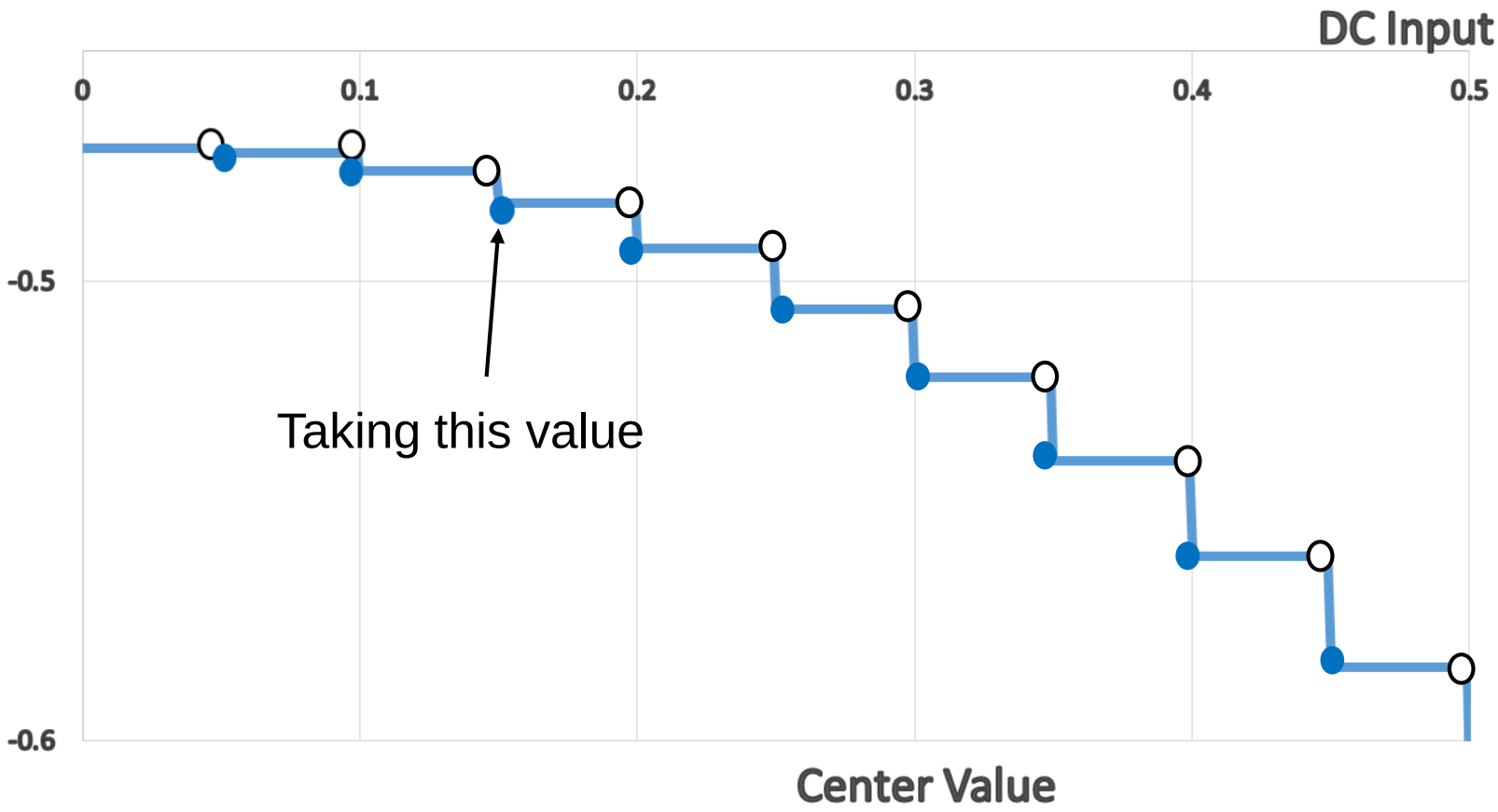
DC = 0.1



Modulator output

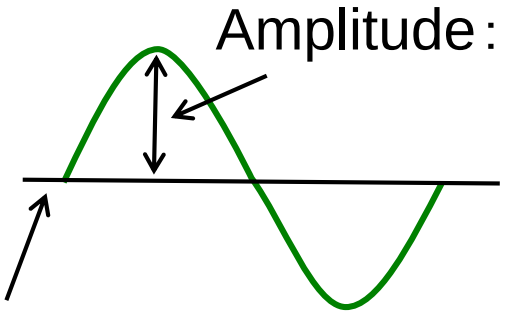


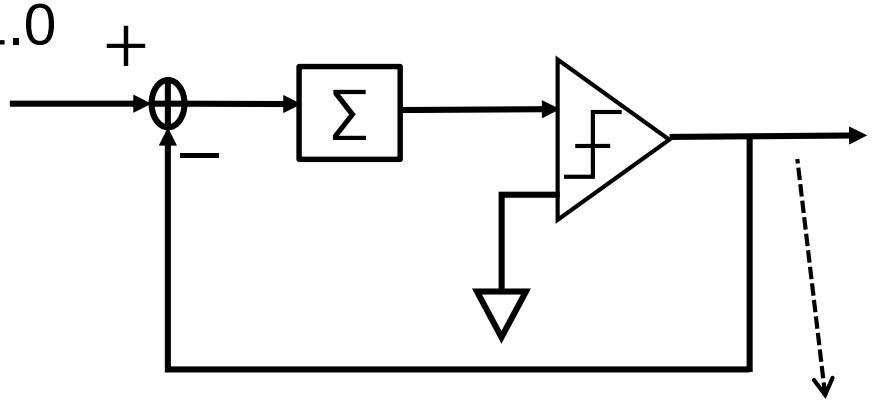
Approximation of Center Value

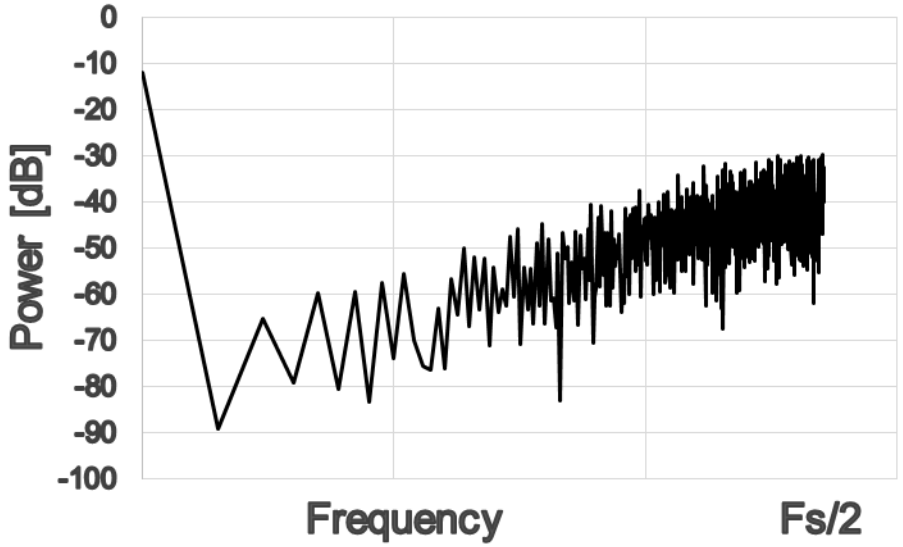


Noise Shaped 10-bit case

Sine Wave







Q & A 発表日:2016/10/28

Q1: FPGA実装で、三角波を正弦波にするとどうなるか。

A1: 正弦波の場合は行っていない。

Q2: FPGAの振幅0.256を、違う値に変えるとどうなるか。

A2: 値を変えた場合は行っていない。

Q3: FPGA実装で、なぜ振幅0.256としたのか。

A3:1周期の三角波に1024点を取っている。1024÷4=256を参考にし、0.001ずつ増加、または減少させ、1周期で三角波が生成できるように設定した。